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(54) Analogue-to-digital converters

(57) An analogue-to-digital converter comprises a plurality of comparators (not shown) coupled to a decoder, Fig 2A (Fig 2B). The decoder has a plurality of decoding stages connected together such that in operation each decoding stage transmits a Gray code output. The Gray code output is achieved by coupling the outputs of each decoding stage to a subsequent decoding stage in a symmetrically folded pattern governed by predefined algorithms. One bit of an output natural binary word is derived from each decoding stage.

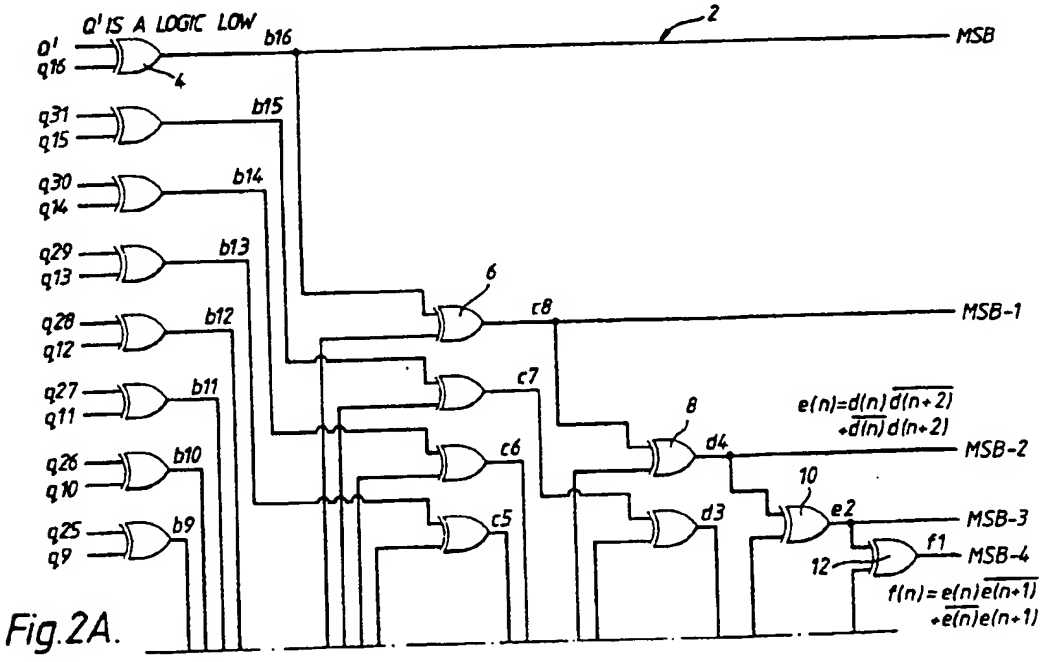

Fig.2A.

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 223 369 A

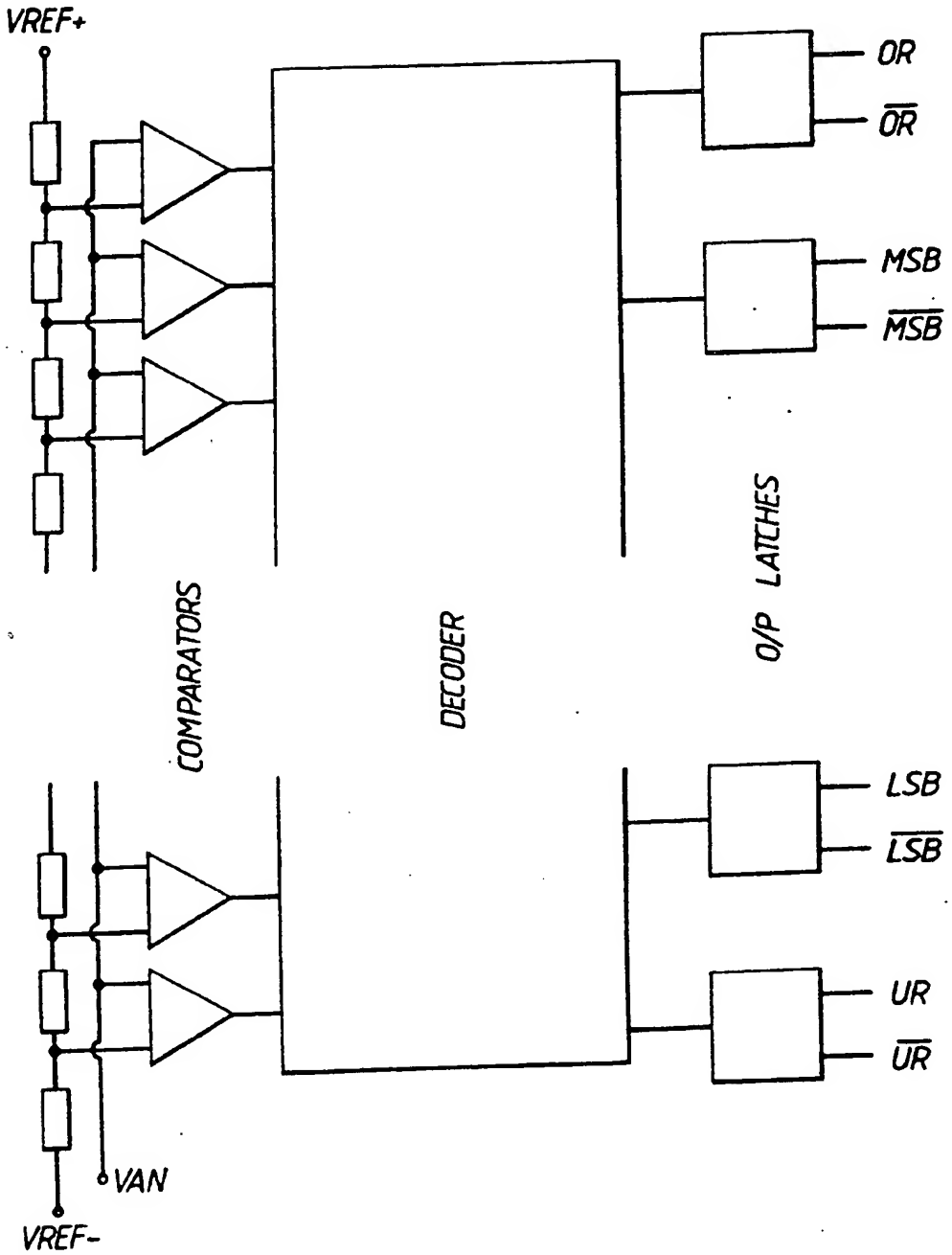
VREF+
OR
$\overline{OR}$
MSB
$\overline{MSB}$
COMPARATORS
DECODER
O/P LATCHES
LSB
$\overline{LSB}$
UR
$\overline{UR}$
VAN
VREF-

Fig.1.

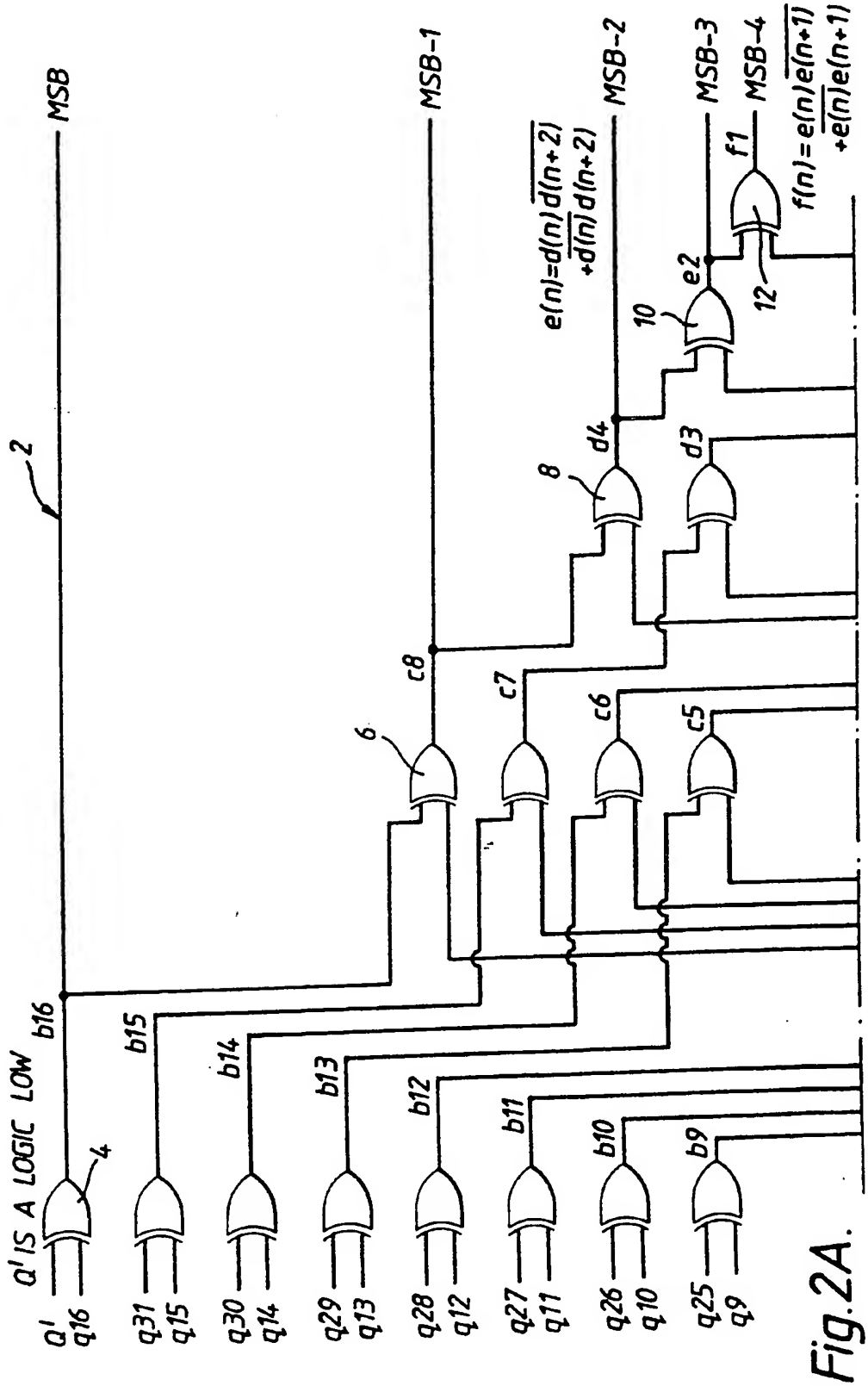
MSB
MSB-1
MSB-2
MSB-3
MSB-4
2
4
6
8
10
12
b16
b15
b14
b13
b12
b11
b10
b9
c8
c7
c6
c5
d4
d3
e2
f1
Q' IS A LOGIC LOW
Q'
q16
q31
q15
q30
q14
q29
q13
q28
q12
q27
q11
q26
q10
q25
q9
e(n)=d(n)d̄(n+2) +d̄(n)d(n+2)
f(n)=e(n)ē(n+1) +ē(n)e(n+1)

Fig.2A.

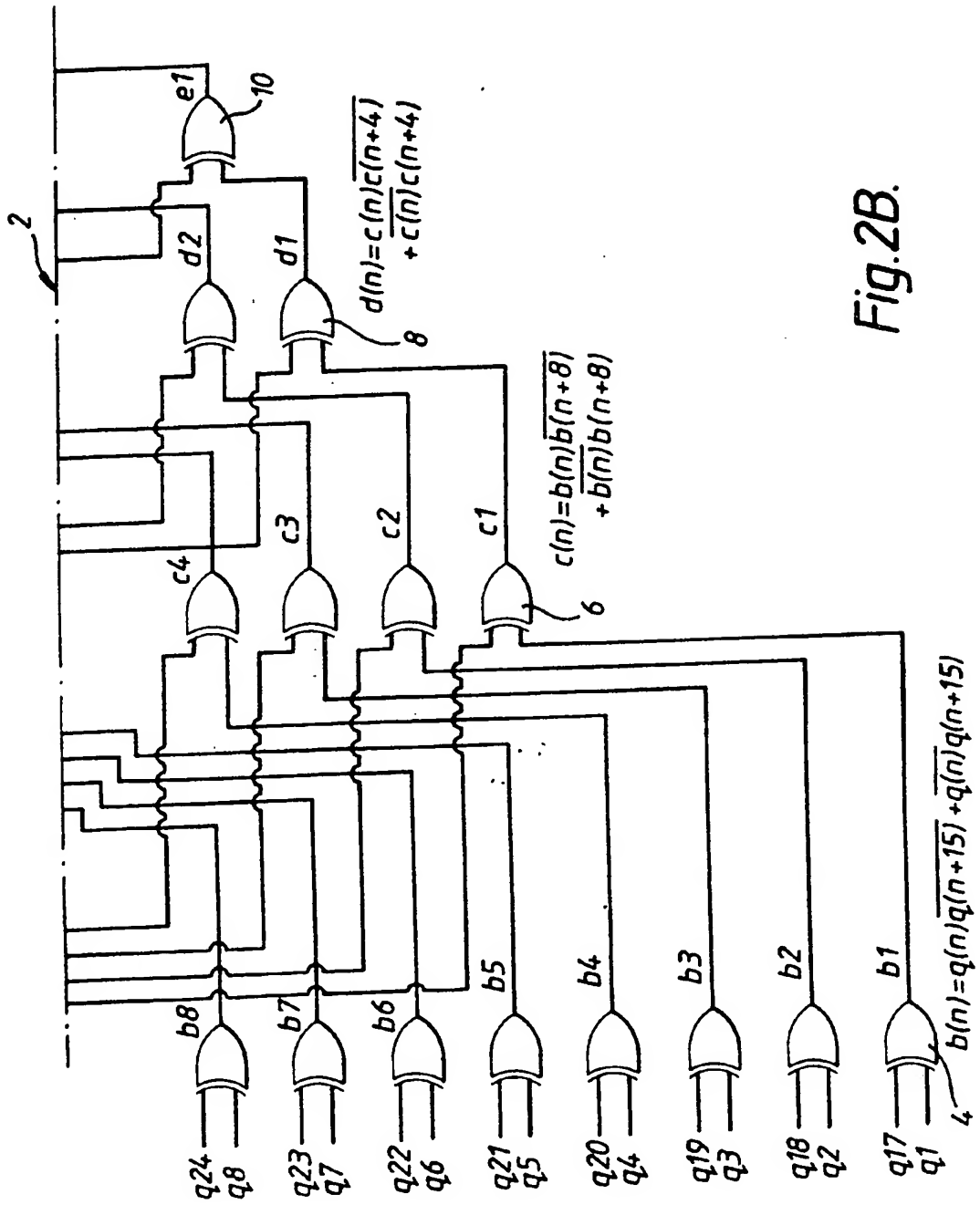
e1
10
2
d2
d1
d(n)=c(n)c(n+4)
+c(n)c(n+4)
8
c4
c3
c2
c1
c(n)=b(n)b(n+8)
+b(n)b(n+8)
6
b8
b7
b6
b5
b4
b3
b2
b1
b(n)=q(n)q(n+15) +q(n)q(n+15)
4
q24
q8
q23
q7
q22
q6
q21
q5
q20
q4
q19
q3
q18
q2
q17
q1

Fig.2B.

$$b(n) = q(n)\overline{q(n+15)} + \overline{q(n)}q(n+15)$$

	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12	b13	b14	b15	b16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0														0
2	1	1	0													0
3	1	1	1	0								0				0
4	1		1	1	0											0
5	1			1	1	0										0
6	1				1	1	0									0
7	1					1	1	0								0
8	1						1	1	0							0
9	1							1	1	0						0
10	1								1	1	0					0
11	1									1	1	0				0
12	1										1	1	0			0
13	1											1	1	0		0
14	1												1	1	0	0
15	1						1							1	1	1
16	1	1													1	1
17	0	1	1													1
18	0	0	1	1												1
19	0		0	1	1											1
20	0			0	1	1										1
21	0				0	1	1									1
22	0					0	1	1								1
23	0						0	1	1							1
24	0							0	1	1						1
25	0								0	1	1					1
26	0		0							0	1	1				1
27	0										0	1	1			1
28	0											0	1	1		1
29	0												0	1	1	1
30	0													0	1	1
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

binary (!)
MSB

Fig.3.

$$c(n) = b(n)\overline{b(n+8)} + \overline{b(n)}b(n+8)$$

	c1	c2	c3	c4	c5	c6	c7	c8
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1						0
3	1		1					0
4	1			1				0
5	1				1			0
6	1					1		0
7	1						1	0
8	1							1
9	0	1						1
10	0		1					1
11	0			1				1
12	0				1			1
13	0					1		1
14	0						1	1
15	0							1
16	0	0	0	0	0	0	0	0
17	1	0						0
18	1	1	0					0
19	1		1	0				0
20	1			1	0			0
21	1				1	0		0
22	1					1	0	0
23	1						1	0
24	1	1	1	1	1	1	1	1
25	0	1						1
26	0	0	1					1
27	0		0	1				1
28	0			0	1			1
29	0				0	1		1
30	0					0	1	1
31	0	0	0	0	0	0	0	1

binary (!)
MSB-1

Fig.4.

$d(n) = c(n)\overline{c(n+4)} + \overline{c(n)}\,c(n+4)$

	d1	d2	d3	d4
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	1	0	0	0
10	1	1	0	0
11	1	1	1	0
12	1	1	1	1
13	0	1	1	1
14	0	0	1	1
15	0	0	0	1
16	0	0	0	0
17	1	0	0	0
18	1	1	0	0
19	1	1	1	0
20	1	1	1	1
21	0	1	1	1
22	0	0	1	1
23	0	0	0	1
24	0	0	0	0
25	1	0	0	0
26	1	1	0	0
27	1	1	1	0
28	1	1	1	1
29	0	1	1	1
30	0	0	1	1
31	0	0	0	1

binary (!)
(MSB-2)

$e(n) = \underline{d(n)}\,\overline{d(n+2)} + \overline{d(n)}\,d(n+2)$

	e(1)	e(2)
0	0	0
1	1	0
2	1	1
3	0	1
4	0	0
5	1	0
6	1	1
7	0	1
8	0	0
9	1	0
10	1	1
11	0	1
12	0	0
13	1	0
14	1	1
15	0	1
16	0	0
17	1	0
18	1	1
19	0	1
20	0	0
21	1	0
22	1	1
23	0	1
24	0	0
25	1	0
26	1	1
27	0	1
28	0	0
29	1	0
30	1	1
31	0	1

binary
(MSB-3)

$f(n) = \underline{e(n)}.\overline{e(n+1)} + \overline{e(n)}.e(n+1)$

	f(1)
0	0
1	1
2	0
3	1
4	0
5	1
6	0
7	1
8	0
9	1
10	0
11	1
12	0
13	1
14	0
15	1
16	0
17	1
18	0
19	1
20	0
21	1
22	0
23	1
24	0
25	1
26	0
27	1
28	0
29	1
30	0
31	1

Fig.5.

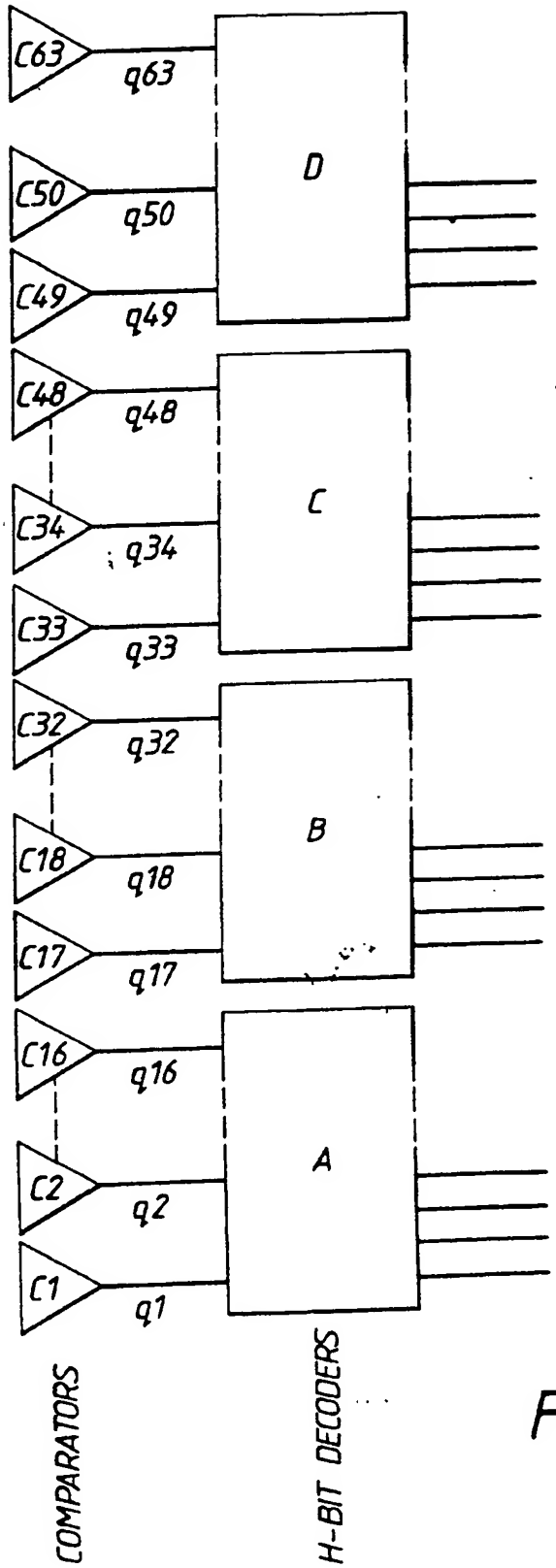
C63
q63
C50
q50
C49
q49
D
C48
q48
C34
q34
C33
q33
C
C32
q32
C18
q18
C17
q17
B
C16
q16
C2
q2
C1
q1
A
COMPARATORS
H-BIT DECODERS

Fig.6.

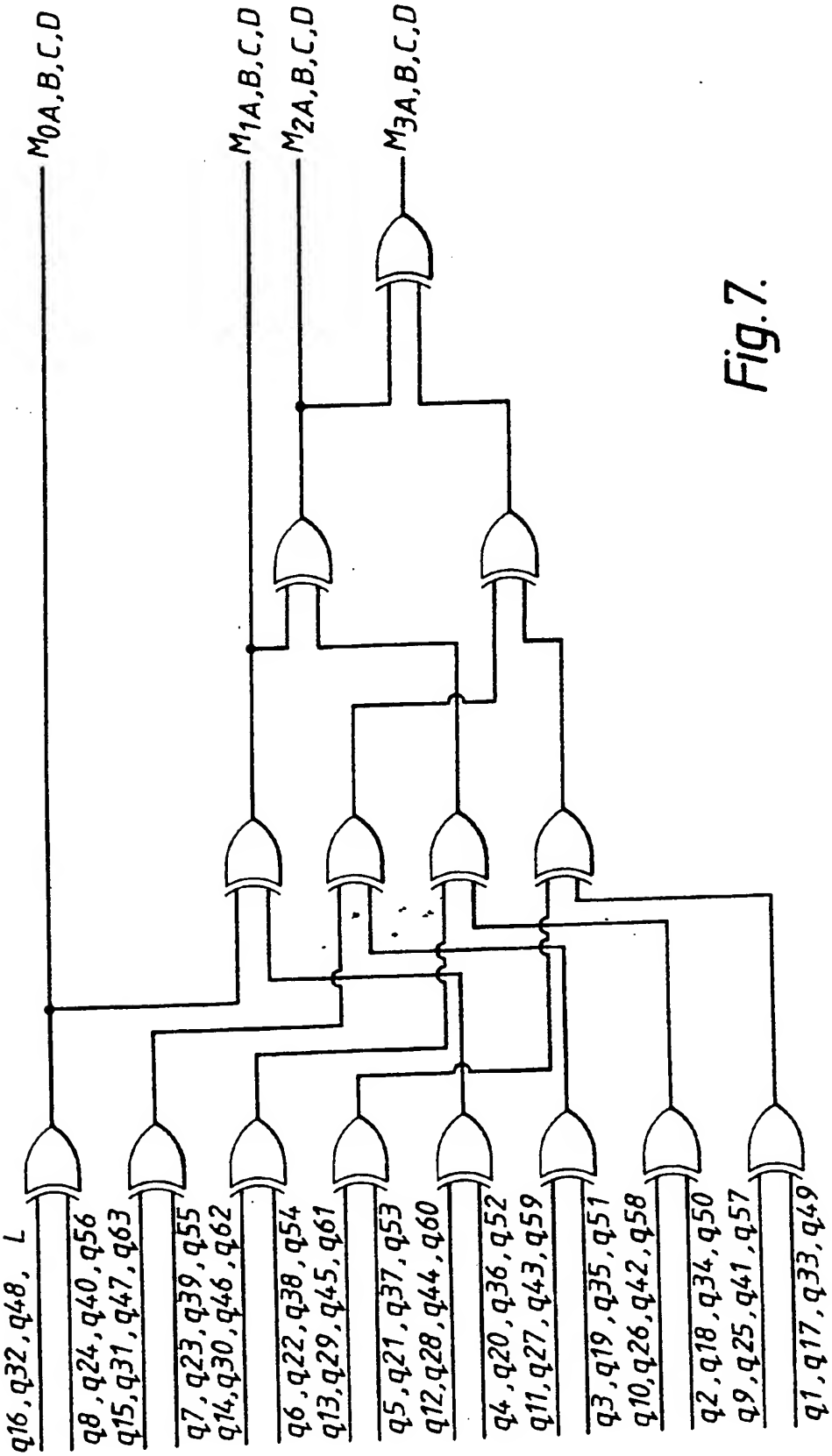
M0A,B,C,D
M1A,B,C,D
M2A,B,C,D
M3A,B,C,D
q16,q32,q48, L
q8,q24,q40,q56
q15,q31,q47,q63
q7,q23,q39,q55
q14,q30,q46,q62
q6,q22,q38,q54
q13,q29,q45,q61
q5,q21,q37,q53
q12,q28,q44,q60
q4,q20,q36,q52
q11,q27,q43,q59
q3,q19,q35,q51
q10,q26,q42,q58
q2,q18,q34,q50
q9,q25,q41,q57
q1,q17,q33,q49

Fig.7.

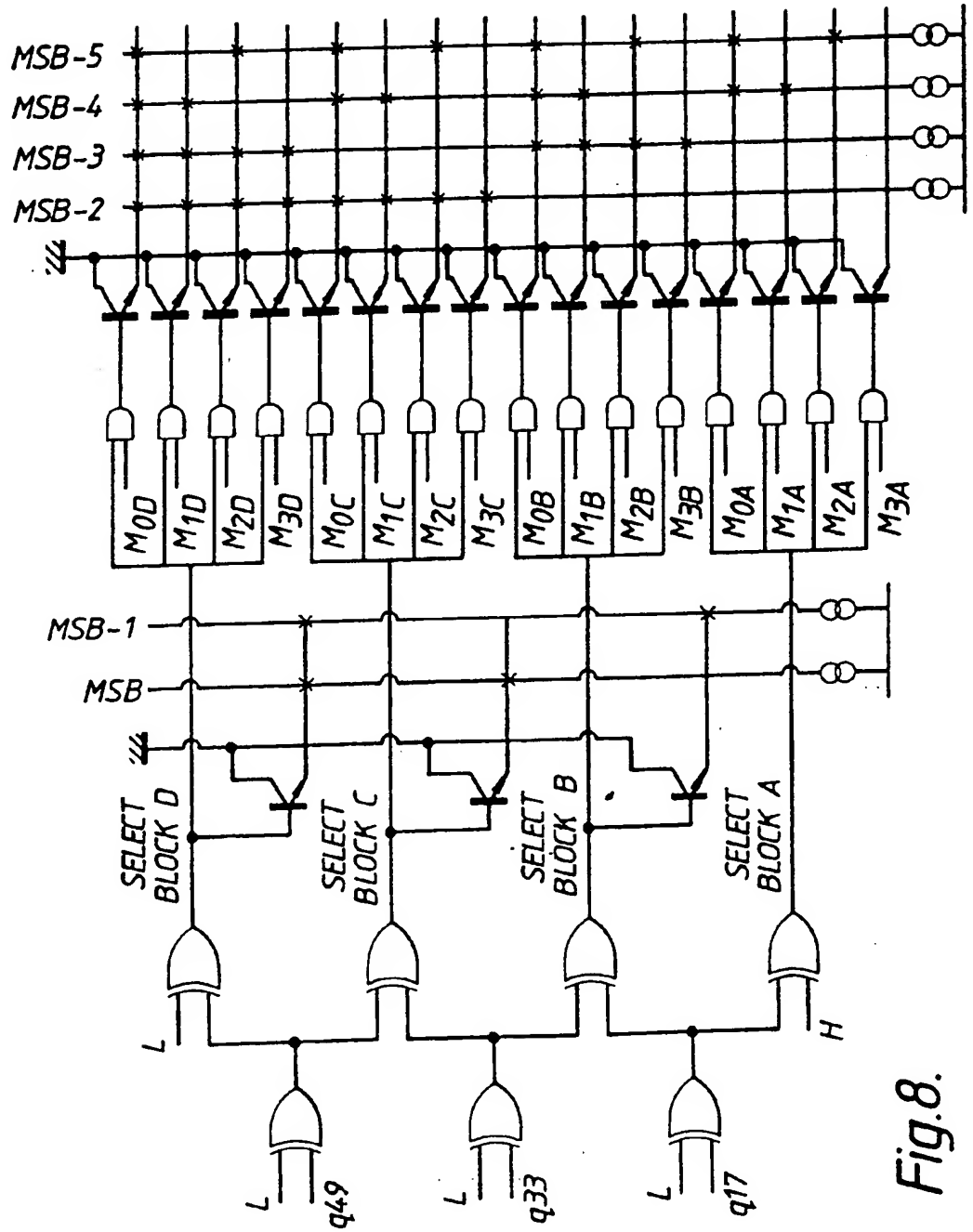
MSB-5
MSB-4
MSB-3
MSB-2
M0D
M1D
M2D
M3D
M0C
M1C
M2C
M3C
M0B
M1B
M2B
M3B
M0A
M1A
M2A
M3A
MSB-1
MSB
SELECT BLOCK D
SELECT BLOCK C
SELECT BLOCK B
SELECT BLOCK A
L
H
L
q49
L
q33
L
q17

Fig.8.

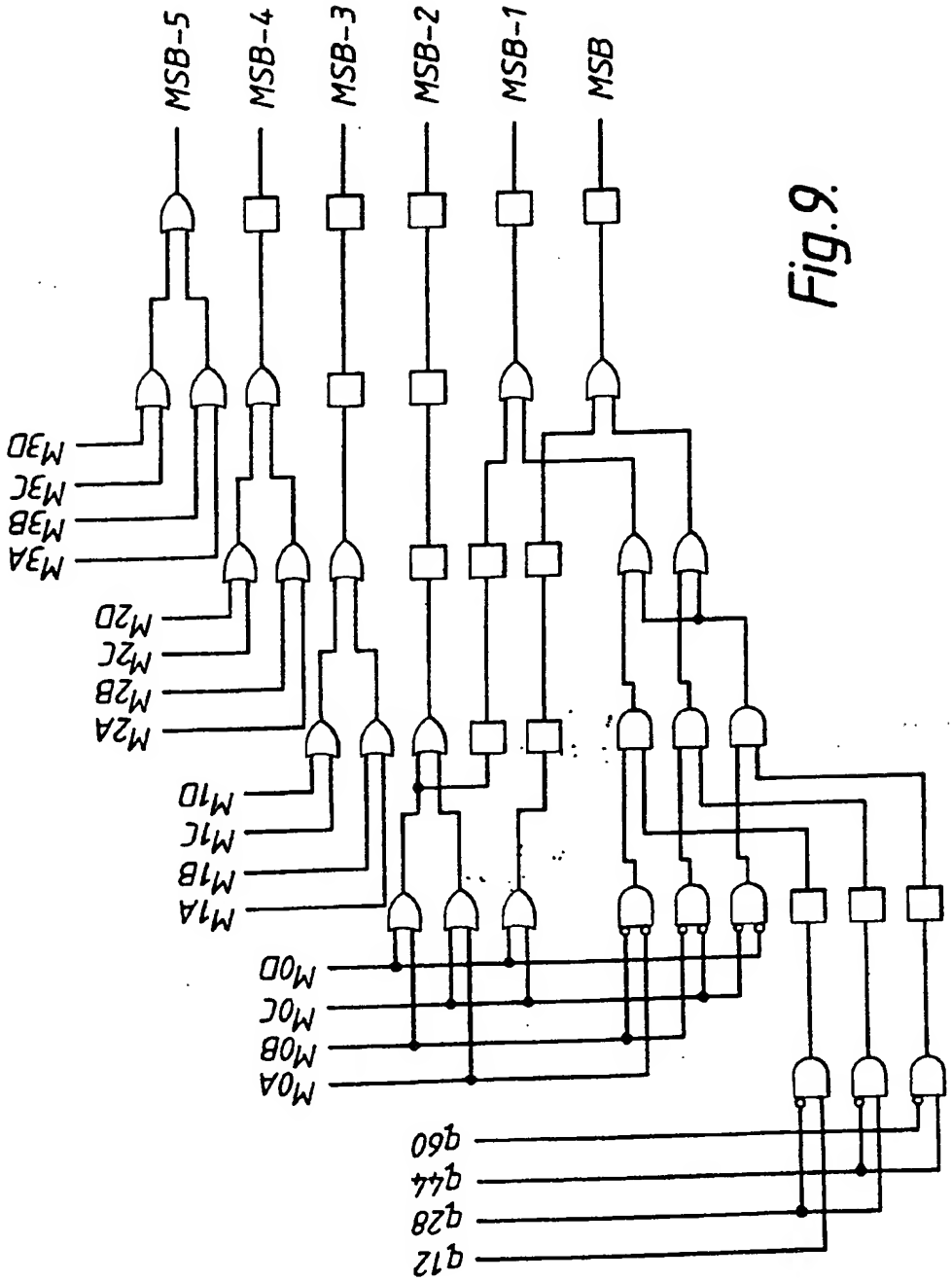
MSB-5
MSB-4
MSB-3
MSB-2
MSB-1
MSB
M3D
M3C
M3B
M3A
M2D
M2C
M2B
M2A
M1D
M1C
M1B
M1A
M0D
M0C
M0B
M0A
q60
q44
q28
q12

Fig.9.

2223369

ANALOGUE-TO-DIGITAL CONVERTERS.

The present invention relates to analogue-to-digital converters.

Figure 1 illustrates a block diagram of a conventional n-bit all-parallel (or "flash") converter. The operation of the device may be described as follows. The 2^n-1 comparators simultaneously and continuously compare the analogue input with 2^n-1 reference values. On receipt of the convert command, the comparators latch the results of these comparisons. All comparators whose reference inputs are less than the value of the analogue input produce an output "high" state. All comparators whose reference inputs are greater than the analogue input will produce an output "low". This is known as a thermometer code. The decoder stage then compresses this 2^n-bit thermometer code into an n-bit code (usually natural binary), which forms the output of the device.

Because each comparator has at its input the difference between a fixed reference value and a continuous analogue signal, there is a finite probability that, on receipt of the convert command, this input will be very close to zero. Under this condition the comparator will be unable to produce an unambiguous output state in the allowed time. This uncertain state can propagate through the decoder and produce gross errors (known as "sparkle" codes) at the output of the converter. There are two methods of reducing the impact of "sparkle" codes on the output signal-to-noise ratio of the ADC.

The first approach is to minimise the probability that a comparator can generate a metastable state. Essentially this requires

that both the gain and bandwidth of the individual comparators be increased as much as possible. Such a technique eventually is very costly in terms of the device power consumption, may be limited by the available manufacturing technology, and in any case, can never reduce the metastable state probability to zero.

The second technique is to develop a decoder structure which is tolerant to the existence of metastable states at its input. This tolerance can be expressed in the following way: a conventional decoder may produce any of the possible 2^n output codes when a metastable state occurs at its input; a more sophisticated decoder under the same conditions will generate either the desired code, or one of the two immediately adjacent to it. An objective of the present invention is to provide an efficient decoder of the latter type.

According to the present invention there is provided an analogue-to-digital converter comprising a plurality of comparators coupled to a decoder having a plurality of decoding stages connected together and adapted such that in operation each decoding stage transmits a Gray code output.

A Gray code is one in which successive words differ only by a single digit.

In one embodiment the analogue-to-digital converter has $2^{(n)}$ comparators the outputs q(i) from which feed $2^{(n-1)}$ logic functions associated with a first decoder stage of the decoder, the outputs q(i) of the logic functions of the first decoder stage being governed by the algorithm:-

$$b(i) = q(i)\,\overline{q(i + 2^{(n-1)})} + q(i + 2^{(n-1)}) \cdot \overline{q(i)}$$

Where i = 1, 2 ----------, $2^{(n-1)}$.

The outputs b(i) of the logic functions of the first decoder stage are connected in a symmetrically folded pattern to the inputs of $2^{(n-2)}$ logic functions of a second decoder stage, the outputs c(i) of the logic functions of the second decoder stage being governed by the algorithm:-

$$c(i) = b(i).\ \overline{b(i + 2^{(n-2)})} + b(i + 2^{(n-2)}) .\ \overline{b(i)}$$

Where $i = 1, 2$ ----------, $2^{(n-2)}$.

In one embodiment the logic functions of each decoder stage are Exclusive-OR functions. In another preferred embodiment the logic functions of the first decoder stage are two-input AND gates having a NOT function on one of the inputs, the logic functions of the second and subsequent decoder stages being Exclusive-OR gates.

In another embodiment of the present invention the decoder is preceded by 2^{n-1} two-input AND gates, the arrangement being such that their outputs will generate in operation either a true thermometer code or one in which only one undecided bit may occur.

The present invention will be described further, by way of example, with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of a conventional all-parallel analogue to digital converter;

Figure 2 is a decoder arrangement according to a first embodiment of the invention;

Figure 3 is a truth table of the Gray code output from the first decoder stage of the decoder of Figure 2;

Figure 4 is a truth table of the Gray code output from the second decoder stage of the decoder of Figure 2; and,

Figure 5 is a series of truth tables of the Gray code output from the third, fourth and fifth decoder stages of Figure 2;

Figure 6 is a block diagram of a 6-bit analogue to digital converter according to an embodiment of the invention;

Figure 7 is a block diagram of one of the four 4-bit decoders employed in the 6-bit analogue to digital converter of Figure 6;

Figure 8 is a decoding arrangement illustrating the manner in which outputs of subsidiary decoders are combined to generate the two most significant bits of a 6-bit output code; and,

Figure 9 is an alternative decoding arrangement to that illustrated in Figure 8.

Referring to Figure 2 there is illustrated a decoder 2 having five decoder stages for a 5-bit analogue-to-digital converter. The analogue-to-digital converter has 2^n comparators (not shown) the outputs of which are labeled in Figure 2 as $q(i) - q^{(2n)}$. The analogue-to-digital converter is 5 bit so there are thirty two outputs from the comparators feeding sixteen Exclusive-OR gates 4.

The outputs from the sixteen Exclusive-OR gates 4 are designated b(1) to b(16) and are governed by a first stage decoder algorithm as follows:-

$$b(i) = q(i).\overline{q(i + 2^{(n-1)})} + q(i + 2^{(n-1)}).\overline{q(i)}$$

Where $i = 1, 2$ ----------, $2^{(n-1)}$.

The outputs b(1) to b(16) of the Exclusive-OR gates 4 are fed in a symmetrically folded pattern to the inputs of eight Exclusive-OR gates 6 defining the second decoder stage. The outputs of the Exclusive-OR gates 6 are represented in Figure 2 by c(1) --- c(8) and are governed by a second stage decoder algorithm as follows:-

$$c(i) = b(i) \cdot \overline{b(i + 2^{(n-2)})} + b(i + 2^{(n-2)}) \cdot \overline{b(i)}$$

Where i = 1, 2 ----------, $2^{(n-2)}$.

The outputs c(1) to c(8) of the Exclusive-OR gates 6 are fed in a symmetrically folded pattern to the inputs of four Exclusive-OR gates 8 defining a third decoder stage. The outputs of the Exclusive-OR gates 8 are represented in Figure 2 by d(1) ------- d(4) and are governed by a third stage decoder algorithm as follows:-

$$d(i) = c(i) \overline{c(i + 2^{(n-3)})} + c(i + 2^{(n-3)}) \cdot \overline{c(i)}$$

Where i = 1, 2 ----------, $2^{(n-3)}$.

The four outputs d(1) --- d(4) of the Exclusive-OR gates 8 are fed in a symmetrically folded pattern to the inputs of two Exclusive-OR gates 10 defining a fourth decoder stage. The outputs of the Exclusive-OR gates 10 are represented in Figure 2 by e(1) and e(2) and are governed by a fourth stage decoder algorithm as follows:-

$$e(i) = d(i) \cdot \overline{d(i + 2^{(n-4)})} + d(i + 2^{(n-4)}) \cdot \overline{d(i)}$$

Where i = 1, 2 ----------, $2^{(n-4)}$.

The outputs e(1) and e(2) of the Exclusive-OR gates 10 are fed to the two inputs of an Exclusive-OR gate 12 defining a fifth decoder stage. The output of the Exclusive-OR gate 12 is shown as f(1).

It will be seen that the number of bits in the output word decreases by two at each stage, and the process continues until the output word is single-bit.

Each decoding stage produces a Gray code output, which is a folded version of the Gray code output of the previous stage. An important feature of this decode scheme is that the "highest" bit in each stage, that is $b(2^{(n-1)})$, $c(2^{(n-2)})$, $d(2^{(n-3)})$, $e(2^{(n-4)})$, and

$f(2^{(n-5)})$ gives successive bits of the output natural binary word. The first decode stage gives the MSB, the second stage give the MSB-1 and so on. Thus an n-bit converter would require n decoding stages with one bit of the output natural binary word becoming available after each stage.

Because the decoding scheme is internally Gray-coded, a metastable condition at the input latch will cause an error of at most 1lsb at the output of the converter.

The decode scheme proposed caters for the condition that the thermometer code output from the input latches does not have a clear transition point, i.e. 1111100000, but rather is of the form 11111X0000, where X is an undetermined state. A further undesirable state which can occur is when the input thermometer code is 11111101000: this situation is less likely than the simple, single undetermined state case. This can be overcome by preceding the decoder described by 2^{n-1} two-input AND gates. The output of these will then generate either a true thermometer code or one in which only one undecided bit may occur.

Figures 3, 4 and 5 illustrate the truth tables of the Gray code outputs from the five decoder stages of the decoder of Figure 2. As will be seen from Figures 3, 4 and 5 the truth tables illustrate a symmetry which determines the symmetrically folded patterns selected for the outputs of a decoder stage feeding respective inputs of the next decoder stage.

Although the present invention has been described with respect to a specific embodiment thereof, it is to be understood that modifications and variations can be made within the scope of the

invention. For example, the Exclusive-OR gates 4 in the first decoder stage can each be replaced by a respective two-input AND gate having a NOT gate on one of its inputs; the subsequent decoding stages retaining their Exclusive-OR gates 6, 8, 10 and 12.

An alternative embodiment of the basic design, useful for alleviating the wiring problems which occur in the decoders of higher resolution ADCs (> 6 bits), is to subdivide the comparators in the ADC into a number of separate blocks, decode the individual blocks using the folding Gray decoder already described and then suitably recombine the outputs of these blocks.

This block sub-division can be done in a number of ways: for example an 8-bit ADC could be decoded as two 7-bit devices, four 6-bit devices, eight 5-bit devices, and so on. For illustrative purposes, a 6-bit ADC with four 4-bit decoders will be discussed in detail. A block diagram of this structure is shown in Figure 6, with the necessary 4-bit decoders shown in Figure 7. As implemented in Figure 7, any decoder block whose inputs do not include the 1 to 0 transition in the comparator thermometer code will output 0000. This will result in ambiguities in the 6-bit output, when the desired output code is any of 000000, 010000, 100000, or 110000. This defect may be overcome in a number of different ways, all of which retain the advantage of the original decoding scheme in terms of insensitivity to input metastable states.

One method of dealing with the 'breaks' between decoding blocks of Figure 6 is to introduce subsidiary decoders which 'bridge' the gaps. In the simplest instance, such a decoder would be the folded Gray decoder already described, appropriate for a notional 1-

bit ADC (comprising thus a single OR gate) for each of the three gaps between main decoder blocks. The outputs of these three gates may be combined, as shown in Figure 8 to generate block select lines, and thus the two most significant bits of the 6-bit output code. These block select lines can be ANDed with the code produced by the appropriate 4-bit decoder, and the outputs of these four 4-bit sections may be wired-ORed to produce the four least significant bits of the 6-bit code.

In an alternative method, which is more efficient (in terms of gate count) but slightly less obvious in operation, outputs from comparators associated with the top half of each of the main decoding blocks can be used with the two most significant bits of the latter to generate the two most significant bits of the 6 bit output code. The bits of lesser significance are obtained by OR-ing the outputs from the four decoder blocks. A diagram of this decoding scheme is shown as Figure 9.

CLAIMS:-

1. An analogue-to-digital converter comprising a plurality of comparators coupled to a decoder having a plurality of decoding stages connected together and adapted such that in operation each decoding stage transmits a Gray code output.

2. An analogue-to-digital converter as claimed in claim 1 wherein the converter has $2^{(n)}$ comparators the outputs q(i) from which feed $2^{(n-1)}$ logic functions associated with a first decoder stage of the decoder, the outputs q(i) of the logic functions of the first decoder stage being governed by the algorithm:-

$$b(i) = q(i).\ \overline{q(i + 2^{(n-1)})} + q(i + 2^{(n-1)}).\ \overline{q(i)}$$

Where i = 1, 2 ----------, $2^{(n-1)}$.

3. An analogue-to-digital converter as claimed in claim 2 wherein the outputs b(i) of the logic functions of the first decoder stage are connected in a symmetrically folded pattern to the inputs of $2^{(n-2)}$ logic functions of a second decoder stage, the outputs c(i) of the logic functions of the second decoder stage being governed by the algorithm:-

$$c(i) = b(i)\ .\ \overline{b(i + 2^{(n-2)})} + b(i + 2^{(n-2)}).\ \overline{b(i)}$$

Where i = 1, 2 ----------, $2^{(n-2)}$.

4. An analogue-to-digital converter as claimed in claim 3 wherein the logic functions of each decoder stage are Exclusive-OR functions.

5. An analogue-to-digital converter as claimed in claim 3 wherein the logic functions of the first decoder stage are two-input AND gates having a Not function on one of the inputs, the logic functions of the second decoder stage being Exclusive-OR gates.

6. An analogue-to-digital converter as claimed in any one of claims 2 to 5 wherein the decoder is preceded by $2^{n}-1$ two-input AND gates, the arrangement being such that their outputs will generate in operation either a true thermometer code or one in which only one undecided bit may occur.

7. An analogue-to-digital converter substantially as hereinbefore described with reference to Figures 2, 3, 4 and 5 of the accompanying drawings.

8. An analogue-to-digital converter substantially as hereinbefore described with reference to Figures 6, 7, and 8 or 9 of the accompanying drawings.

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